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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,597	01/15/2002	Shunpei Yamazaki	07977-290001/US5432	4657

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EXAMINER	
DOLAN, JENNIFER M	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,597	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-68 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 9,10,12-14,16,45,46,48,53,54,56-58,60-62 and 64 is/are allowed.

6)☒ Claim(s) 1-8,10,15,17-44,47,49-52,55,59,63 and 65-68 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 2, 3, 6, 7, 10, 11, 14, 15, 18, 19, 2, 23, 26, 27, 30, 31, 34, 35, 38, 39, 42, 43, 46, 47, 50, 51, 54, 55, 58, 59, 62, 63, 66, and 67 are objected to because of the following informalities: In line 1, "any one of" should be omitted. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 3, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43, 47, 51, 55, 59, 63, and 67 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. All of the recited claims require the connection wiring line and the pixel electrode to be formed from the same conductive film. The specification and figures, however, do not teach or show the connection wiring line and pixel electrode formed from the same conductive film, and in fact, suggest that they are formed of different films (see page 8, lines 1-9, and figures 5D, 7A, and 7B of the present application).

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 3 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 3 and 7 recite the limitation "the pixel electrode". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 4, 5, 8, 17, 20, 21, 24, 25, 28, 29, and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,462,722 to Kimura et al.

Regarding claims 1 and 5, Kimura discloses a light emitting device comprising a thin film transistor (121) and a capacitor storage (123, formed by 113 and 114; column 3, lines 28-30), wherein the capacitor storage has a connection wiring line (113 along with portion connecting source/drain of 121 to 113, equivalent to part 427 in figure 14d), a capacitance wiring line (114), and an insulating film (figure 6a, or equivalently, 43 in figure 14d) formed between the connection wiring line and the capacitance wiring line, the connection wiring line being formed on an interlayer insulating film that covers a gate electrode (portion 427 formed on insulator over 111) of the thin film transistor (figure 6a), wherein the connection wiring line is connected to a source or a drain region of the thin film transistor (figure 6a). Regarding claim 5,

Kimura further discloses that the connection wiring line overlaps an active layer of the TFT (figures 6a and 6b).

Regarding claims 17, 21 25, and 29, Kimura discloses a light emitting device comprising a source line (112), a power supply line (114), a switching thin film transistor (121), a driving thin film transistor (122), a capacitor storage (123, formed from 113 and 114), and an organic light emitting diode (131), wherein the switching TFT has a source region and a drain region (figure 6a, crosshatched regions at 121), one of which is connected to a source line (figure 6a), and the other of which is connected to a gate electrode of the driving TFT (through 113; see figures 2 and 6a; column 3, lines 23-26, 36-39) through a connection wiring line (113 and portion in figure 6a equivalent to part 427 in figure 14d); wherein the driving TFT has a source region and a drain region, one of which is connected to the power supply line (114, figure 6a) and the other of which is connected to a pixel electrode (115) of the organic LED (figure 6a), wherein the connection wiring line is formed on an interlayer insulating film that covers a gate electrode of the switching TFT (figure 6a; portion equivalent to 427 in figure 14d is formed above the interlayer insulating film). Regarding claims 17 and 25, Kimura discloses that the capacitor storage (123) has the connection wiring line (113 and portion equivalent to 427), a capacitance wiring line (114), and an insulating film formed between the connection wiring line and the capacitance wiring line (figure 6a). Regarding claims 21 and 29, Kimura discloses that the capacitor storage has a capacitance electrode (113) and the power supply line (114), and an insulating film formed between the capacitance electrode and the power supply line, the capacitance electrode being formed of the same conductive film as the gate electrode of the

driving TFT (figure 14b). Regarding claims 25 and 29, Kimura discloses that the connection wiring line overlaps an active layer of the switching TFT (figures 6a and 6b).

Regarding claims 4, 8, 20, 24, 28, and 32, Kimura discloses an organic light emitting diode display comprising the specified light emitting device (column 1, lines 30-40; column 10, lines 29-34).

8. Claims 65 and 68 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,521,913 to Murade.

Regarding claim 65, Murade discloses a light emitting device comprising a plurality of pixels (figure 1, all pixels along row G1) each having a TFT (30) and a capacitor storage (70), wherein all of the capacitor storages of the plurality of pixels share one capacitance wiring line (3b, figure 1), wherein each of the capacitor storages of the plurality of pixels has a connection wiring line (80) and an insulating film (81), the connection wiring line being formed on an interlayer insulating film (81) that covers a gate electrode (3a) of the TFT (30; figures 2 and 3), the insulating film being formed between the connection wiring film and the capacitance wiring line (figure 3), wherein the connection wiring line is connected to a drain region (1c) of the TFT, and wherein the capacitance wiring line overlaps an active layer of the TFT of each of the plurality of pixels (figures 8 and 12).

Regarding claim 68, Murade discloses that the appliance is a notebook personal computer or a mobile computer (column 36, lines 26-40).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 41, 44, 49, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. in view of Murade.

Regarding claims 41 and 49, Kimura discloses a light emitting device comprising a source line (112), a power supply line (114), a switching thin film transistor (121), a driving thin film transistor (122), a first capacitor storage (123, formed from 113 and 114), and an organic light emitting diode (131), wherein the switching TFT has a source region and a drain region (figure 6a, crosshatched regions at 121), one of which is connected to a source line (figure 6a), and the other of which is connected to a gate electrode of the driving TFT (through 113; see figures 2 and 6a; column 3, lines 23-26, 36-39) through a connection wiring line (113 and portion in figure 6a equivalent to part 427 in figure 14d); wherein the driving TFT has a source region and a drain region, one of which is connected to the power supply line (114, figure 6a) and the other of which is connected to a pixel electrode (115) of the organic LED (figure 6a), wherein the connection wiring line is formed on an interlayer insulating film that covers a gate electrode of the switching TFT (figure 6a; portion equivalent to 427 in figure 14d is formed above the interlayer insulating film), wherein the first capacitor storage (123) has the connection wiring line (113 and portion equivalent to 427), a capacitance wiring line (114), and an insulating film formed between the connection wiring line and the capacitance wiring line (figure

6a). Regarding claim 49, Kimura discloses that the connection wiring line overlaps an active layer of the switching TFT (figures 6a and 6b).

Kimura fails to disclose a second capacitor storage.

Murade discloses a second capacitor storage (70a), having a capacitance electrode (3b), a semiconductor layer (1f), and a second insulating film (2) formed between the capacitance electrode and the semiconductor layer, the capacitance electrode being formed of the same conductive film as the gate electrode (3a) of the TFTs (figure 5, step 10), and the semiconductor layer being formed at the same time as the active layers of the TFTs are formed (figure 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the light emitting device of Kimura to include the second capacitor as taught by Murade. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide a second capacitor with the claimed properties, because Murade teaches that it is desirable to provide a fine pixel pitch for enhanced picture quality, but as the device size is decreased, it is difficult to obtain sufficient storage capacitance in a reduced area (see Murade, column 2, lines 31-53). Murade further teaches that an arrangement using stacked first and second capacitors, with the second capacitor formed using a semiconductor region and a metal layer on the same level as the gate electrodes greatly increases the storage capacitance per area occupied in the pixel (see Murade, column 12, lines 19-39; column 21, lines 1-10).

Regarding claims 44 and 52, Kimura discloses an organic light emitting diode display comprising the specified light emitting device (column 1, lines 30-40; column 10, lines 29-34).

11. Claims 33, 36, 37, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. in view of U.S. Patent No. 6,441,829 to Blalock et al.

Regarding claims 33 and 37, Kimura discloses a light emitting device comprising a source line (112), a power supply line (114), a switching thin film transistor (121), a driving thin film transistor (122), a capacitor storage (123, formed from 113 and 114), and an organic light emitting diode (131), wherein the switching TFT has a source region and a drain region (figure 6a, crosshatched regions at 121), one of which is connected to a source line (figure 6a), and the other of which is connected to a gate electrode of the driving TFT (through 113; see figures 2 and 6a; column 3, lines 23-26, 36-39) through a connection wiring line (113 and portion in figure 6a equivalent to part 427 in figure 14d); wherein the driving TFT has a source region and a drain region, one of which is connected to the power supply line (114, figure 6a) and the other of which is connected to a pixel electrode (115) of the organic LED (figure 6a), wherein the connection wiring line is formed on an interlayer insulating film that covers a gate electrode of the switching TFT (figure 6a; portion equivalent to 427 in figure 14d is formed above the interlayer insulating film). Regarding claim 33, Kimura discloses that the capacitor storage (123) has the connection wiring line (113 and portion equivalent to 427), a capacitance wiring line (114), and an insulating film formed between the connection wiring line and the capacitance wiring line (figure 6a). Kimura further discloses that a drain current of the driving thin film transistor is inputted to the source line (112, via switching TFT 121; see figure 1), and the drain current flows into the organic light emitting diode (131; figure 1). (Regarding claim 37, Kimura discloses that the capacitor storage has a capacitance electrode (113) and the power supply line (114), and an insulating film formed between the capacitance electrode and the power supply

line, the capacitance electrode being formed of the same conductive film as the gate electrode of the driving TFT (figure 14b).

Kimura is silent as to the nature of the drive circuitry for the source line.

Blalock discloses that the source line is controlled by an analog video signal (column 1, lines 43-50; figure 3a).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the source line of Kimura is controlled by an analog video signal. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an analog video signal for driving the OLED, because doing so allows the display device to be used for miniature video and graphics display devices (Blalock, column 1, lines 13-56).

Regarding claims 36 and 40, Kimura discloses an organic light emitting diode display comprising the specified light emitting device (column 1, lines 30-40; column 10, lines 29-34).

12. Claims 2, 6, 18, 22, 26, and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. in view of U.S. Patent No. 6,121,652 to Suzawa (cited by applicant).

Kimura fails to disclose that the insulating films are formed by anodization.

Suzawa discloses that the insulating films (layer above 417) are formed by anodization (column 2, lines 52-58; column 8, lines 31-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulating film of Kimura, so that it is an anodic oxide, as taught by Suzawa. The rationale is as follows: One of ordinary skill in the art at the time the invention was

made would have been motivated to use an anodic oxide, because doing so simplifies the fabrication procedure, by eliminating the need for depositing a separate dielectric layer.

13. Claims 34 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. in view of Blalock et al. as applied to claims 33 and 37 above, and further in view of Suzawa.

Kimura fails to disclose that the insulating films are formed by anodization.

Suzawa discloses that the insulating films (layer above 417) are formed by anodization (column 2, lines 52-58; column 8, lines 31-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulating film of Kimura as modified by Blalock, so that it is an anodic oxide, as taught by Suzawa. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an anodic oxide, because doing so simplifies the fabrication procedure, by eliminating the need for depositing a separate dielectric layer.

14. Claims 42 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. in view of Murade, as applied to claims 41 and 49 above, and further in view of Suzawa et al.

Kimura fails to disclose that the insulating films are formed by anodization.

Suzawa discloses that the insulating films (layer above 417) are formed by anodization (column 2, lines 52-58; column 8, lines 31-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulating film of Kimura as modified by Murade, so that it is an anodic oxide, as taught by Suzawa. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an anodic oxide, because doing so simplifies the fabrication procedure, by eliminating the need for depositing a separate dielectric layer.

15. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murade in view of Suzawa et al.

Murade fails to disclose that the insulating films are formed by anodization.

Suzawa discloses that the insulating films (layer above 417) are formed by anodization (column 2, lines 52-58; column 8, lines 31-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulating film of Murade, so that it is an anodic oxide, as taught by Suzawa. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an anodic oxide, because doing so simplifies the fabrication procedure, by eliminating the need for depositing a separate dielectric layer.

Allowable Subject Matter

16. Claims 9, 10, 12-14, 16, 45, 46, 48, 53, 54, 56-58, 60-62, and 64 are allowed.

17. The following is an examiner's statement of reasons for allowance:

Regarding claims 9, 10, 12-14, and 16, the prior art of record, considered as a whole, fails to teach or suggest a light emitting device with a connection wiring line formed on an interlayer insulating film that covers a gate electrode and a capacitance wiring line formed on the same interlayer insulating film on which a pixel electrode is formed.

U.S. Patent No. 6,462,722 to Kimura discloses the connection wiring line formed on an interlayer insulating film that covers a gate electrode, but the corresponding capacitance wiring line is formed below the connection wiring line, rather than on the same level as the pixel electrode.

U.S. Patent No. 6,121,652 to Suzawa teaches a capacitance wiring line on the same level as the pixel electrode, but the connection wiring line is not formed on the insulating film covering the gate electrode, nor is it connected to the source or drain region of the TFT. Thus, there is no motivation or feasible way to combine these references to anticipate claims 9 and 13.

Regarding claims 45, 46, 48, 53, 54, and 56, the prior art of record fails to teach or suggest both a first capacitor storage with connection and capacitance wiring lines as specified, and a second capacitor storage with a capacitance electrode and the power supply line as specified.

U.S. Patent No. 6,521,913 to Murade discloses a device with two storage capacitors, but neither one is connected to the power supply line, and there is neither a motivation to connect either capacitor to the power supply line nor a way to feasibly do so without fundamentally changing the nature of the device disclosed by Murade.

Regarding claims 57, 58, 60-62, and 64, the prior art of record fails to disclose a third storage capacitor, as specified. Murade discloses the use of two storage capacitors, but there is no motivation or obvious means of adding a third storage capacitor to the disclosed device.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,492,778 to Segawa, U.S. Patent No. 5,747,930 to Utsugi, U.S. Patent No. 6,351,078 to Wang et al., U.S. Patent Publication No. 2002/0070913 to Kimura et al. and U.S. Patent No. 6,057,647 to Kurosawa et al. disclose pixel arrangements using a plurality of TFTs and a single storage capacitor.

b. U.S. Patent No. 6,229,506 to Dawson et al. discloses a circuit diagram for a pixel containing two storage capacitors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd
April 3, 2003

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800